Flow control on IEEE 802.3x switch

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Based on chapter 8 :
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Half or full duplex?

- LANs are intrinsically half-duplex:
  - Only a station at a time can transmit

- Switching strongly reduces shared medium role:
  - Often transmissive medium become point to point: only a station is linked to switch

- Point to point transmissive media can be full-duplex:
  - Both stations can transmit at same time
  - Trasmissions take place on different physical channels
Full duplex and 802.3x standard

- 802.3x standard define full duplex functioning modes
- Modes are negotiated between equipment and stored in the 4th register

Technology Ability Field

<table>
<thead>
<tr>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>D5</th>
<th>D6</th>
<th>D7</th>
<th>D8</th>
<th>D9</th>
<th>D10</th>
<th>D11</th>
<th>D12</th>
<th>D13</th>
<th>D14</th>
<th>D15</th>
</tr>
</thead>
<tbody>
<tr>
<td>rsvd</td>
<td>rsvd</td>
<td>rsvd</td>
<td>rsvd</td>
<td>FD</td>
<td>HD</td>
<td>PS1</td>
<td>PS2</td>
<td>rsvd</td>
<td>rsvd</td>
<td>rsvd</td>
<td>RF1</td>
<td>RF2</td>
<td>Ack</td>
<td>NP</td>
<td></td>
</tr>
</tbody>
</table>

- 0 1: Half Duplex
- 1 0: Full Duplex

<table>
<thead>
<tr>
<th>D0</th>
<th>D1</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>No error, Link OK</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>Offline</td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>Link Failure</td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>Auto-Negotiation Error</td>
<td></td>
</tr>
</tbody>
</table>
Full duplex functioning modes

- MAC CSMA-CD is no longer used
  - Packets are immediately transmitted by Ethernet stations without sensing the channel
- Always used on switch-switch links, less on switch-station links
- Special transceiver are needed because collision mustn’t be detected:
  - ordinary transceiver send a collision signal to the interface when contemporary TX and RX activities are present
- Distance between two Ethernet full-duplex station
  - depends on transmissive channel features only
  - is independent from collision diameter domain
Half and full duplex transceivers

DO = Data Output   DI = Data Input   CI = Collision Input
Distance limits

- In full-duplex Ethernet:
  - 100 m for telephone twisted pair
  - 2 Km for 62.5/125 μm multimode optic fiber
  - in case of monomode optic fiber and transceiver equipped with category II laser (as in FDDI and Fast-Ethernet), the maximum distance can be 50 Km
  - in Gigabit Ethernet with high power laser:
    - 75 Km for monomode fiber
    - 100 Km for dispersion-shift monomode fiber
Flow control: IEEE 802.3x

Define:

- MAC IEEE 802.3 necessary changes in order to support Full-Duplex mode
- flow control mechanism for Full-Duplex links
- available for all Ethernet networks (10/100/1000 Mb/s)
- Mandatory for Gigabit Ethernet, optional for Ethernet and Fast Ethernet
OSI model and IEEE 802.3x

- IEEE 802.3x introduce a sublayer (MAC Control) between MAC 802.3 and higher sublayer (Bridge Relay Entity, LLC, ...)

ISO/OSI model

<table>
<thead>
<tr>
<th>Application</th>
<th>Presentation</th>
<th>Session</th>
<th>Transport</th>
<th>Network</th>
<th>Data Link</th>
<th>Physical</th>
</tr>
</thead>
</table>

LAN 802 sublayers

- LLC sublayer
- MAC Control (optional)
- MAC - Media Access Control
Flow control

- Control flow mechanism is defined in IEEE 802.3x:
  - The device willing to stop transmission send a PAUSE packet in multicast to every partner concerned in the transmission
    - packet contains the amount of time (number of slot time) that each partner must stop transmission
    - the times can be extended or aborted by sending another PAUSE packet
## PAUSE packet

<table>
<thead>
<tr>
<th>6 octets</th>
<th>Destination Address (01-80-C2-00-00-01)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 octets</td>
<td>Source Address</td>
</tr>
<tr>
<td>2 octets</td>
<td>Length/Type = 8808</td>
</tr>
<tr>
<td>2 octets</td>
<td>OpCode = 00-01 (PAUSE)</td>
</tr>
<tr>
<td>2 octets</td>
<td>Pause_time (pause-quanta)</td>
</tr>
<tr>
<td>42 octets</td>
<td>PAD (all 0s)</td>
</tr>
<tr>
<td>4 octets</td>
<td>FCS</td>
</tr>
</tbody>
</table>
Pause time

- Pause_time field: number of pause-quanta (from 0 to 65535) which indicate the pause time
  - pause-quanta = 512 bit time
  - speed equal or less than 100 Mb/s
    - T-Pause in bit time = pause-quanta * 512
  - Speed greater than 100 Mb/s
    - T-Pause in bit time = pause-quanta * 512 * 2
IEEE 802.3x: flow control modes

- Two flow controls mechanism:
  - **asymmetric** mode
    - only one equipment send pause packet, the other just receive the packet and stop transmitting
  - **symmetric** mode
    - both equipment at link’s edge can transmit and receive the pause packet
Flow Control negotiation

- Flow control negotiation using Burst FLP (Fast Link Pulse) coding
  - initially sent by both partners in link’s parameter negotiation phase
Flow control: FLP Reg.4 encoding

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<td>RF1</td>
<td>RF2</td>
<td>Ack</td>
<td>NP</td>
</tr>
</tbody>
</table>

- **0 0**: No error, Link OK
- **0 1**: Offline
- **1 0**: Link Failure
- **1 1**: Auto-Negotiation Error

- **0 0**: No Pause
- **0 1**: Asymmetric Pause to link partner
- **1 0**: Symmetric Pause
- **1 1**: Symmetric Pause e Asymmetric Pause (tipo “Both”) to local device
# Flow control: FLP Reg.4 encoding

## Register 4: Auto-Negotiation Advertisement Register

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
<th>Default</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Next Page</td>
<td>Constant 0 = page transmissione with primary capacity</td>
<td>0</td>
<td>RO</td>
</tr>
<tr>
<td>14</td>
<td>Reserved</td>
<td>Reserved. Must be set to 0</td>
<td>0</td>
<td>RO</td>
</tr>
<tr>
<td>13</td>
<td>Remote Fault</td>
<td>1 = malfunctioning at link’s opposite side 0 = nessun malfunzionamento</td>
<td>0</td>
<td>RW</td>
</tr>
<tr>
<td>12:5</td>
<td>Technology Ability Field</td>
<td>8 bit field containing info on technologies’ specific functionalities identified by selector field</td>
<td>00101111</td>
<td>RW</td>
</tr>
<tr>
<td>4:0</td>
<td>Selector Field</td>
<td>5 bit field which identifies the kind of message sented for the negotiation. In the Intel 82559 circuitry this field is read-only and contains 00001b value which stand for IEEE 802.3 standard.</td>
<td>00001</td>
<td>RO</td>
</tr>
<tr>
<td>Local Device</td>
<td>Link Partner</td>
<td>Local Device resolution</td>
<td>Link Partner resolution</td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>--------------</td>
<td>-------------------------</td>
<td>-------------------------</td>
<td></td>
</tr>
<tr>
<td>Bit - PS1</td>
<td>Bit - PS2</td>
<td>Bit - PS1</td>
<td>Bit - PS2</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Don’t care</td>
<td>Don’t care</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX &amp; RX</td>
<td>TX &amp; RX</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Don’t care</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
</tr>
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<td>0</td>
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<td>Disable PAUSE</td>
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<td></td>
<td>TX &amp; RX</td>
<td>TX &amp; RX</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Don’t care</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
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<td></td>
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<td>TX &amp; RX</td>
<td></td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enable PAUSE TX</td>
<td>Enable PAUSE RX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>RX</td>
<td>TX</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Don’t care</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX &amp; RX</td>
<td>TX &amp; RX</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enable PAUSE</td>
<td>Enable PAUSE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX &amp; RX</td>
<td>RX</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX &amp; RX</td>
<td>TX &amp; RX</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enable PAUSE RX</td>
<td>Enable PAUSE TX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE RX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX</td>
<td>RX</td>
<td></td>
</tr>
<tr>
<td>Both Sym &amp; Asym Pause</td>
<td>Both Sym &amp; Asym Pause</td>
<td>Enable PAUSE TX</td>
<td>Enable PAUSE RX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable PAUSE</td>
<td>Disable PAUSE</td>
<td></td>
</tr>
</tbody>
</table>

Asymmetric Pause

Both Sym & Asym Pause

Symmetric or Both

Don’t care

Disable PAUSE

TX & RX

Enable PAUSE

TX & RX

Disable PAUSE

RX

Enable PAUSE

TX

Disable PAUSE

RX
Switch’s flow control: output buffer

- Switch with output buffer and input port connection
  - output buffer saturation cause the sending of Pause on input port linked with traffic flow
  - solution not implemented by vendors because has more drawback than benefit
  - Pause packet on link between two switches penalize also the traffic flows which don’t congest output buffers

- Vendors’ solution:
  - switch blocks transmission on port if it receive the Pause packet, but it can’t send the pause packet
Asymmetric flow control
Symmetric flow control

Interface’s buffer

Pause sending

Pause threshold

Buffer saturation

Pause

Sending

To the CPU

interface’s buffer

Pause sending

Pause threshold

Buffer saturation

Pause

Sending

To the CPU
Symmetric flow control
Output Buffer port 4

- Pause threshold
- Buffer saturation

Interface’s buffer

- Pause threshold
- Buffer saturation

To the CPU

100 Mb/s

PC-7

PC-8

PC-5

Novembre 2002
Pause

Interface’s buffer

Pause threshold
Buffer saturation

Pause sending

Output Buffer port 4

PC-7

100 Mb/s

PC-5

Pause

100 Mb/s

Pause threshold
Buffer saturation

To the CPU

To the CPU

PC-8
Interface’s buffer

Output Buffer port 4

Pause threshold

Buffer saturation

PC-7

Pause sending

PC-8

Pause

PC-5

To the CPU

100 Mb/s

1

2

3

4

Novembre 2002
Interface’s buffer

Pause threshold

Buffer saturation

Output Buffer port 4

100 Mb/s

100 Mb/s

PC-7

PC-8

PC-5

To the CPU

Pause threshold

Buffer saturation
Interface’s buffer

Pause threshold

Buffer saturation

To the CPU

100 Mb/s

1

2

3

4

PC-7

PC-8

PC-5

To the CPU

Interface’s buffer

Pause threshold

Buffer saturation

100 Mb/s
Symmetric flow control

Asymmetric flow control

Sym. or Both Pause

Both Pause

Sym. or Both Pause

Asym. Pause

Both Pause

Sym. or Both Pause

Asym. Pause

Fast station

Slow station
Blocks all flows!
Flow control on switch with input buffer

- If an input buffer met is saturation because of input port congestion, it send a Pause packet in the concerned port
  - If switching matrix is blocking
  - If exist contention on output ports
    - No output buffer
    - Output buffer are full

- If switching matrix is congested, the event unleash the sending of Pause packet on all ports
  - Pause packet sending occurs only on switch with blocking matrix
Symmetric flow control
Symmetric flow control
Realistical approach on switch with output buffer

- Asymmetric flow control is enabled only on switch-station connections
  - make up temporary congestions on input buffers of station’s network interfaces
  - not an ideal solution, but can be a good deal in certain traffic condition